To: D. Thompson, T. Johnson
From: D. Sheppard
Re: ACD FREE Modification Proposal
Date: 3-5-2004
Cc: R. Baker, J. Odom

Summary:

On 1/15/04, a Problem Report was written against the ACD electronics. A fix to the problem was proposed in a previous report, dated 2/12/04. This report is found at:

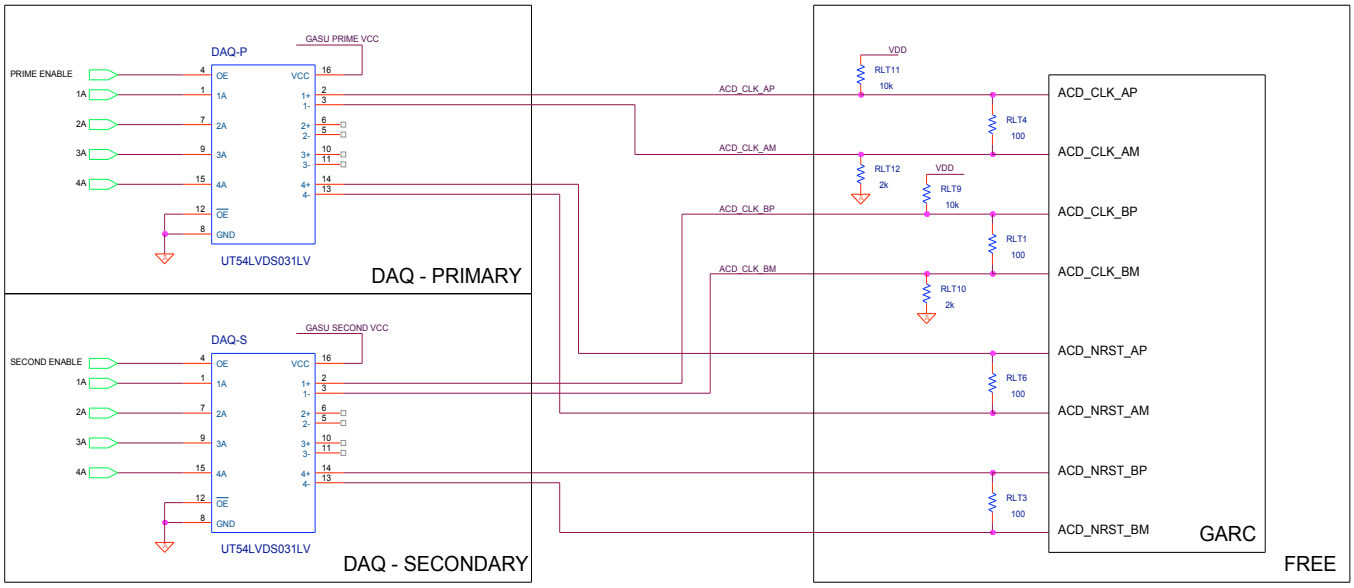
http://lhea-glast.gsfc.nasa.gov/acd/electronics/free/FREE_Board_Reset_Fix.pdf

This is a follow-on to that report, incorporating a modification suggested by Oren Milgrome.

Schematic of the Proposed Circuit Modifications:

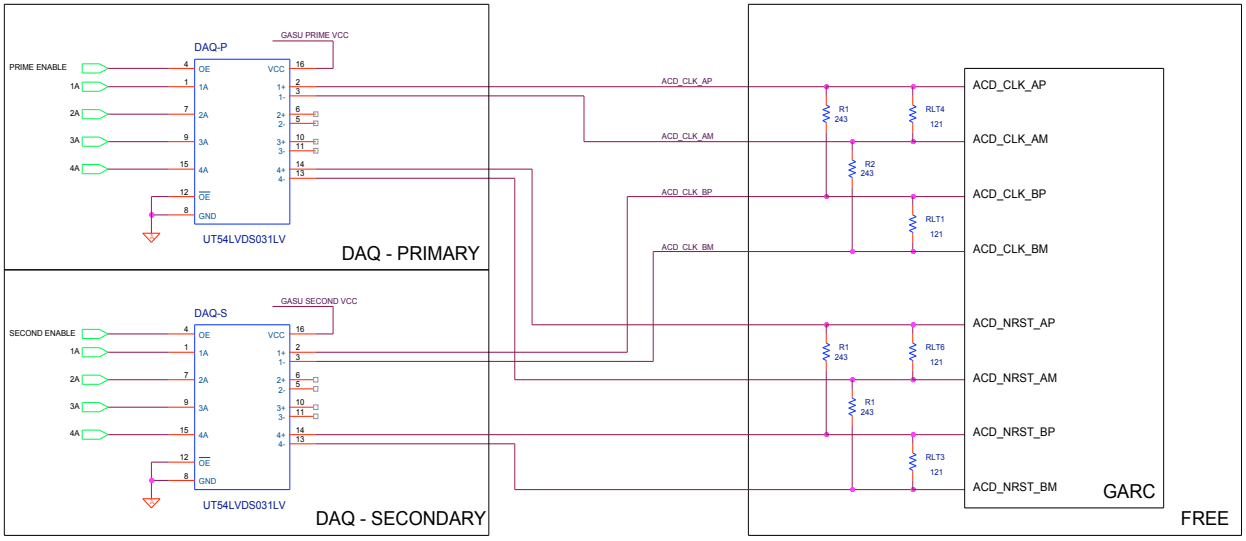
The proposed modification involves cross-strapping the clock and reset inputs to allow a portion of the transmitted signal to be seen by both sets of receivers. The circuit as it presently exists on the FREE card is shown below:

Present Circuit



The schematic of the proposed fix to the flight FREE cards is shown below:

Proposed Circuit

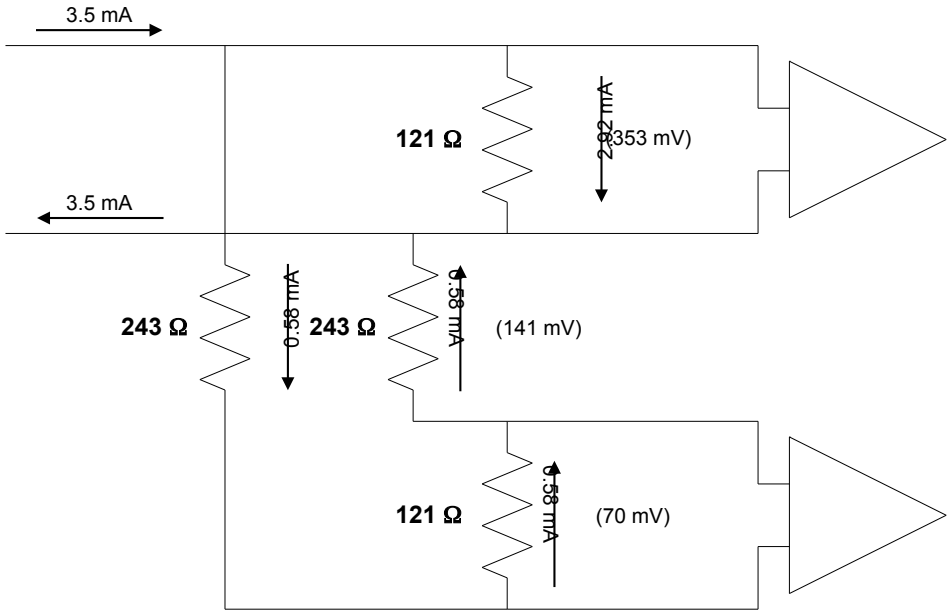


Total termination impedance using the 121 Ω resistors at the receiver inputs and the 243 Ω cross-strapping resistors is:

$$Z = \frac{(121)(243+121+243)}{121+243+121+243} = 100.9\Omega$$

which is close to the desired 100Ω termination.

The calculated signal amplitudes based on nominal LVDS currents are shown below:



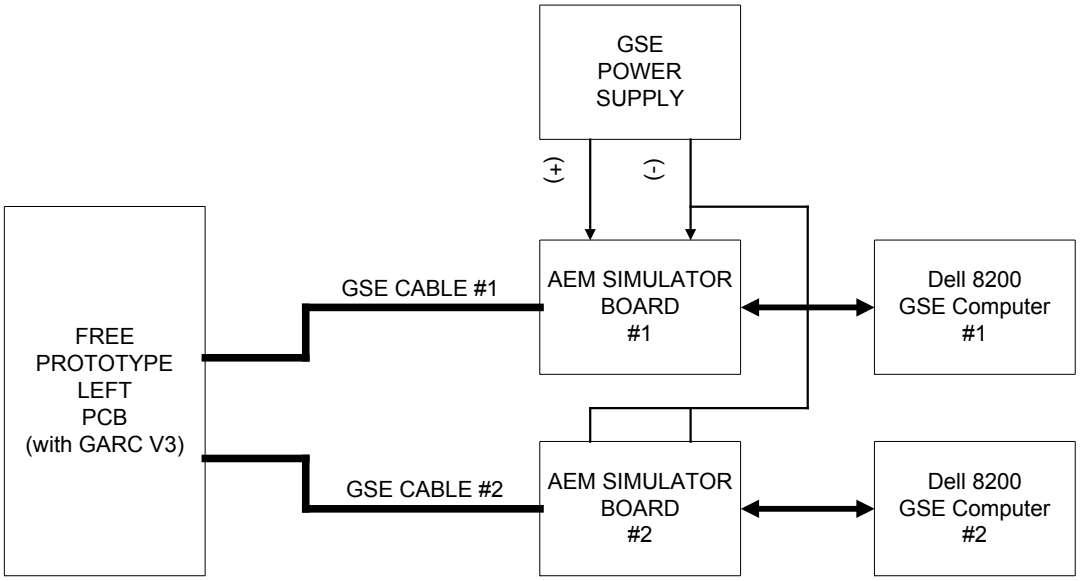
The primary (powered) receiver maintains the ~ 350 mV signal across the 121Ω resistor with 2.92 mA of (nominal) current. 580 μA current is shunted through the 243 ohm resistors and the redundant (unpowered) receiver. This provides ~ 70 mV of difference across the unpowered receiver, which is enough to toggle the GARC receiver in the absence of cabling reflections.

In this proposal, cabling reflections from the unterminated, unpowered driver side are quite significant with flight length cables. At the nominal 20 MHz clock rate, this fix does not function reliably. SLAC has agreed to configure the GASU to drop the clock rate to approximately 1 MHz for 1 second at FREE board turn on to mitigate this problem. At the 1 MHz rate, the reflections do not hinder operation and the FREE card redundant (unpowered) receiver will receive clocks reliably (which is the goal of this modification). After 1 second, SLAC will command the GASU to return the FREE card clock to the nominal 20 MHz rate for operations.

The proposed change is to be made on both the clock and the reset signal paths. If both the primary and redundant clock receivers can be active, it is necessary to ensure the reset level is held inactive.

Data taken in the Lab:

This modification has been tested on the bench with a setup that is similar to the flight configuration (we will retest with the GASU when it becomes available). The test setup was as follows:

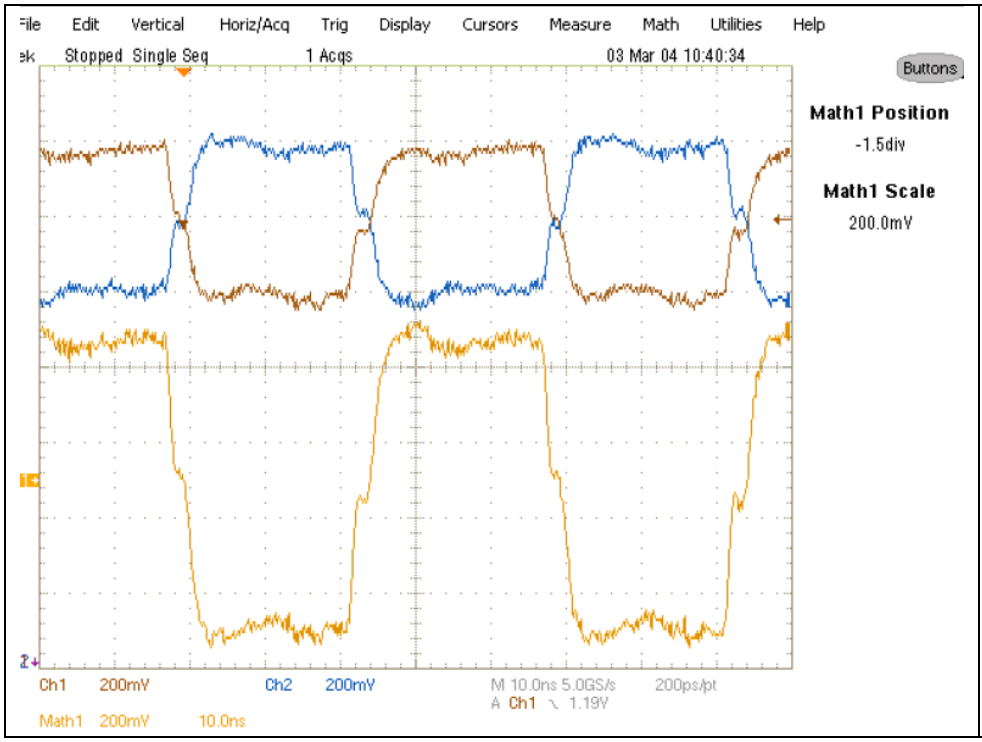


In this setup, AEM simulator board #2 was kept powered off with the power leads shorted together and tied to ground. This is to simulate the redundant (unpowered) DAQ card in the GASU.

The following configurations were tested:

Active FREE Port	Inactive FREE Port	Cable on Active Port
JP1	JS2	Long
JP1	JS2	Short
JS2	JP1	Long
JS2	JP1	Short

All configurations are functional. Minimal differences in oscilloscope traces were noted due to cabling length. Commanded resets function nominally at 20 MHz.



FREE PL Board Test
3-3-04

Freq = 20 MHz

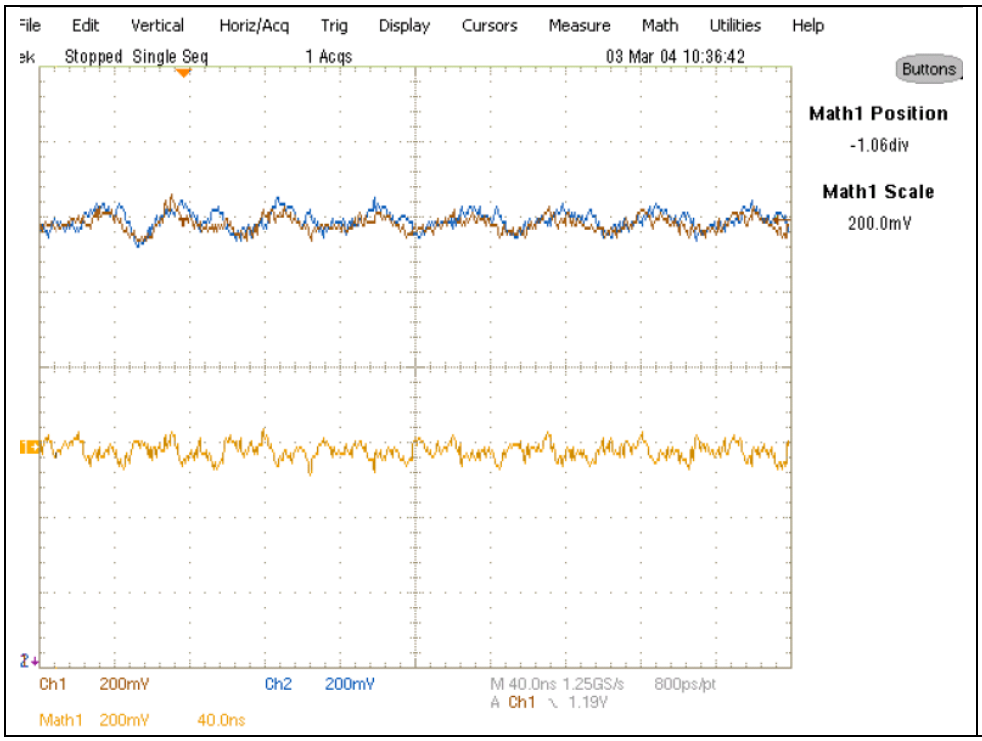
Probes at RLT4 powered receiver

Long cable on powered driver, short on unpowered driver

Timebase 10 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 100 mV/div is the differential seen by driver

Powered receiver, 20 MHz, Differential signal is ~ 700 mV



FREE PL Board Test
3-3-04

Freq = 20 MHz

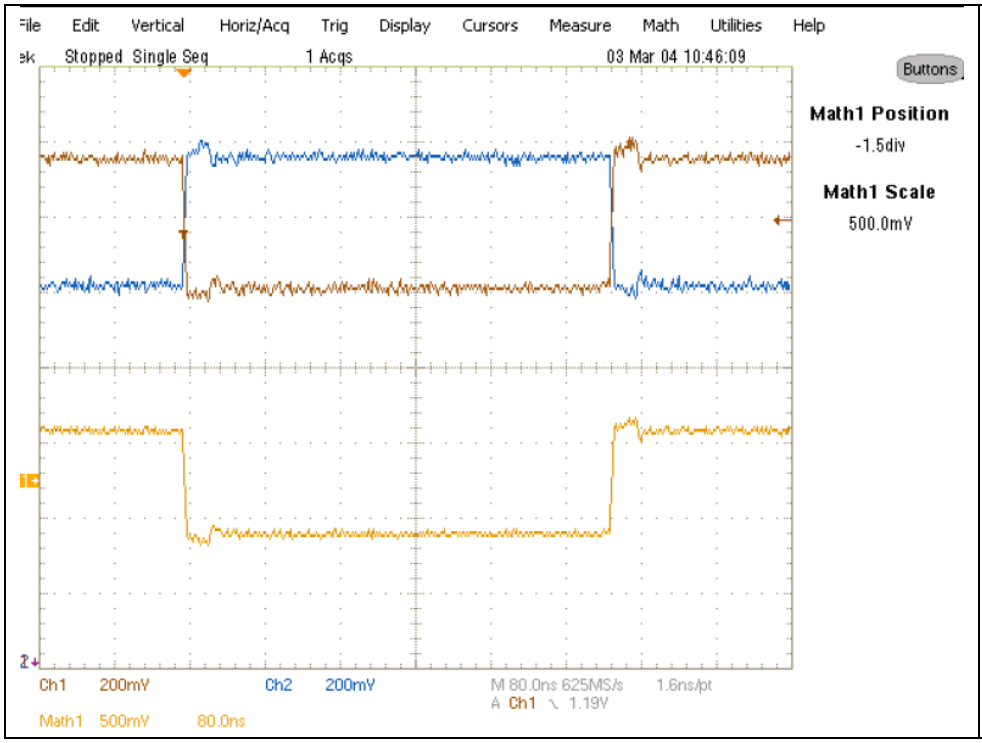
Probes at RLT1
unpowered receiver

Short cable on
powered driver, long
on unpowered driver

Timebase 40 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 200 mV/div
is the differential
seen by receiver

Powered receiver, 20 MHz. Implementation has no margin at 20 MHz as tested.



FREE PL Board Test
3-3-04

Freq = 1 MHz

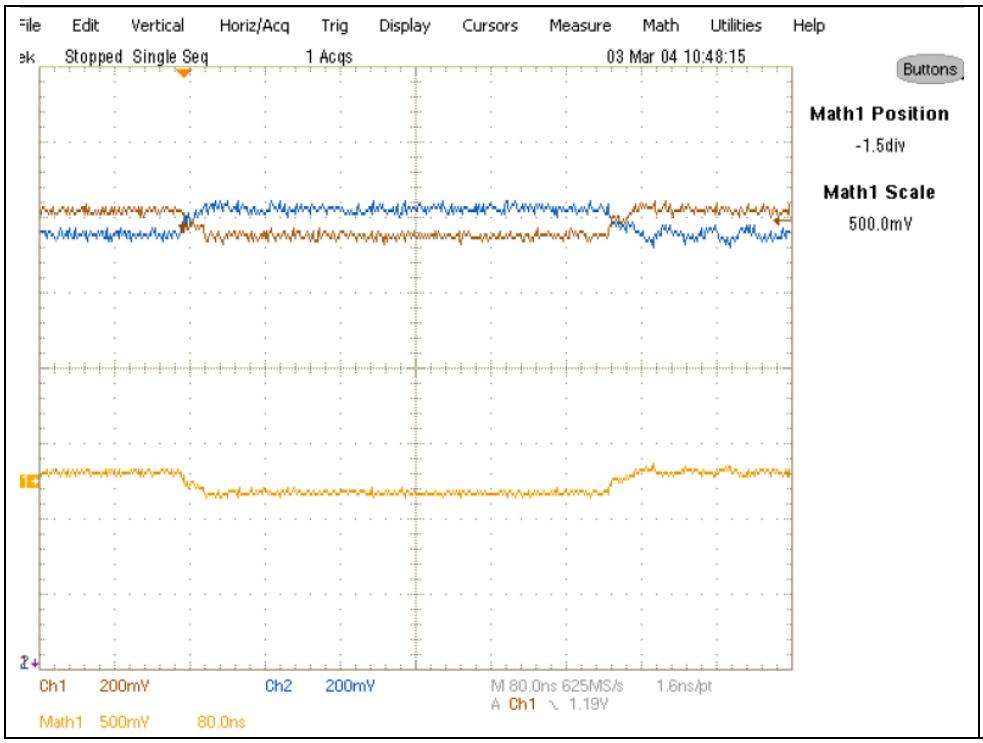
Probes at RLT4
powered receiver

Long cable on
powered driver, short
on unpowered driver

Timebase 80 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by receiver

Powered side, 1 MHz, Differential signal is ~ 700 mV



FREE PL Board Test
3-3-04

Freq = 1 MHz

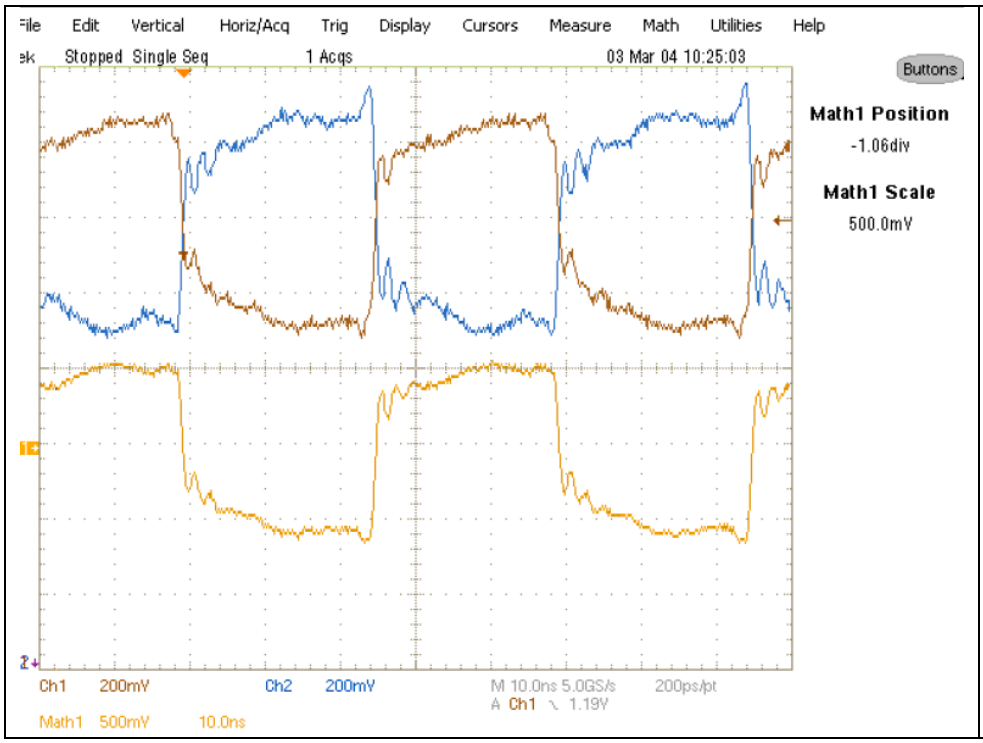
Probes at RLT1
unpowered receiver

Long cable on
powered driver, short
on unpowered driver

Timebase 80 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by driver

Unpowered receiver, 1 MHz, Differential signal is ~ 150 mV



FREE PL Board Test
3-3-04

Freq = 20 MHz

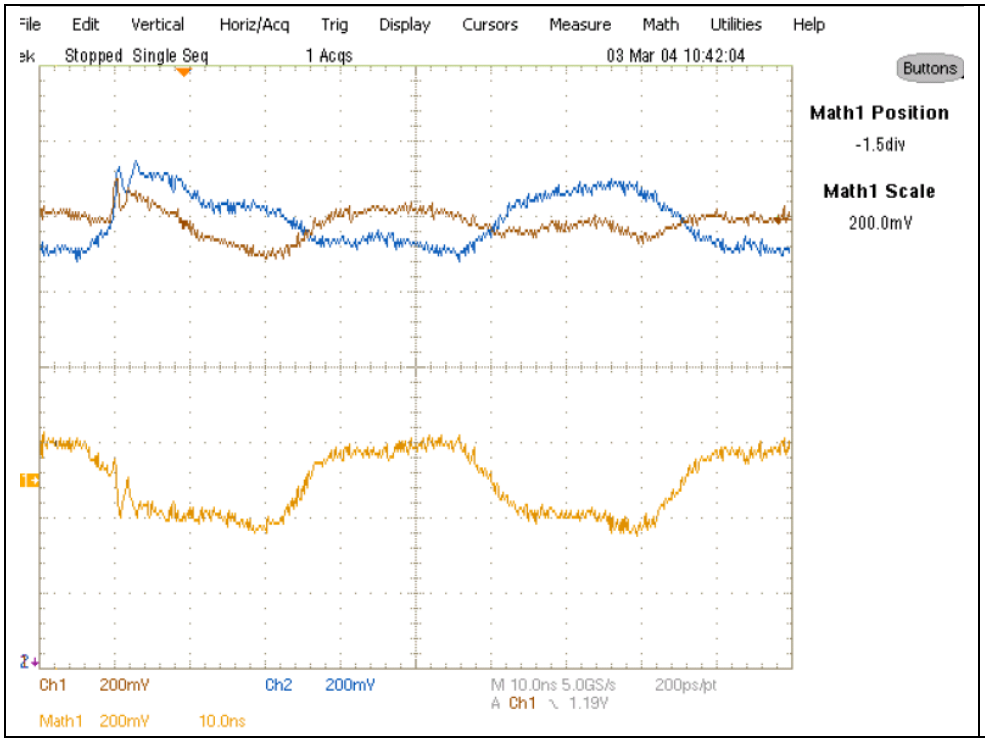
Probes at R44
powered driver

Long cable on
powered driver, short
on unpowered driver

Timebase 10 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by driver

Powered driver, 20 MHz, Differential signal is ~ 700 mV



FREE PL Board Test
3-3-04

Freq = 20 MHz

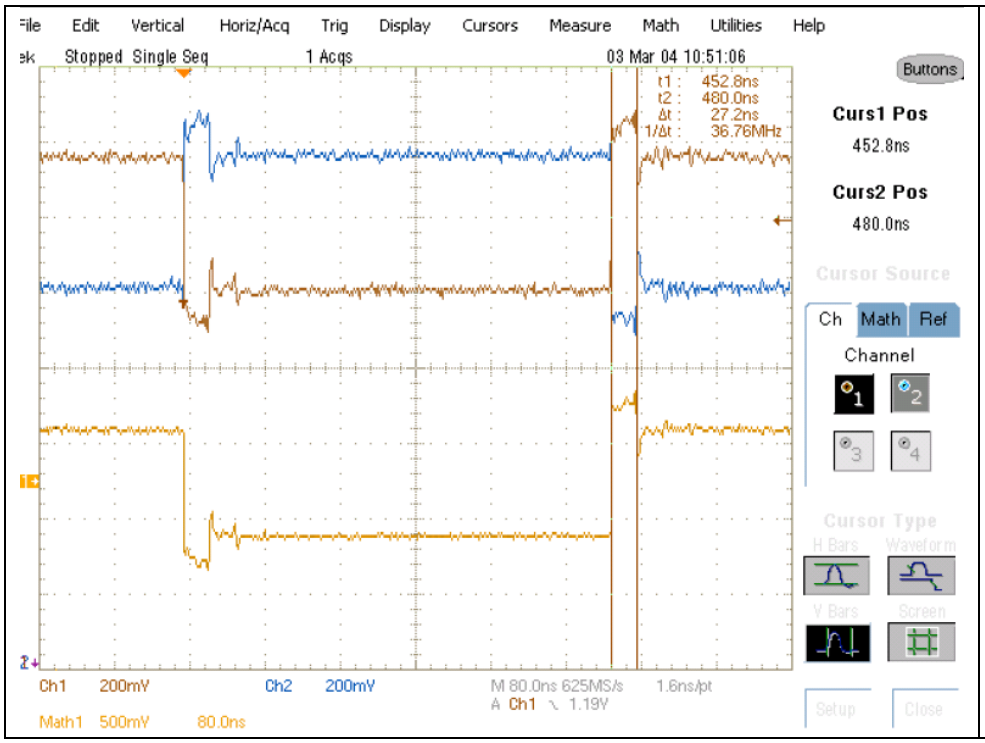
Probes at R44
unpowered driver

Long cable on
powered driver, short
on unpowered driver

Timebase 10 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 200 mV/div
is the differential
seen by driver

Unpowered driver, 20 MHz



FREE PL Board Test
3-3-04

Freq = 1 MHz

Probes at R44
powered driver

Long cable on
powered driver, short
on unpowered driver

Timebase 80 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by driver

Powered driver, 1 MHz. Cable reflections cause discontinuity at 27 ns.